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(54) Planar type semiconductor device with a high breakdown voltage.

(57) A planar type semiconductor device with a high breakdown voltage has a diffusion region (2) of P type formed in a semiconductor layer (1) of N type, at least one guard ring region (7a, 7b) of P type provided surrounding the diffusion region, and an insulating film (3) covering a given portion on a surface of the semiconductor layer of N type. The planar type semiconductor device is further comprised of a first field plate (9a) kept at the potential equal to that of the diffusion region, and a second field plate (9b) which is provided on the insulating film outside a guard ring region and is kept at the potential equal to that of the guard ring region.

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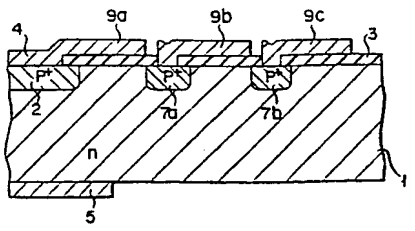

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Planar type semiconductor device with a high breakdown voltage

The present invention relates to a planar type semiconductor device, and more particularly to a planar type semiconductor device with a high breakdown voltage having a field plate and a guard ring.

In general, a breakdown voltage of a planar type semiconductor device is lower than that of a mesa type semiconductor device. The reason for this is that, in the planar type semiconductor device, an electric field is concentrated mainly at a PN junction in the surface area of a semiconductor substrate, so that a breakdown voltage at the PN junction in the surface area is lower than that at the PN junction in the interior of the substrate. It is well known that a field plate or a guard ring is used for a means for improving a breakdown voltage of the planar type semiconductor device. A structure of a PN diode with a field plate, for example, is illustrated in Fig. 1 and a structure of a PN diode with a guard ring is illustrated in Fig. 2. In Figs. 1 and 2, reference numeral 1 designates an N type semiconductor substrate, 2 a P^+ type diffusion area formed on the surface of the substrate 1, 3 an insulating film of SiO_2, for example, 4 an anode electrode, 5 a cathode electrode. In Fig. 1, a field plate 6 integral with an anode electrode 4 is provided on an insulating

film formed outside a P^+ type diffusion area 2. When an inverse bias voltage -V is applied to an anode electrode 4 of the device shown in Fig. 1, a depletion layer formed in the substrate 1 takes a shape as indicated by a broken line. The field plate 6 weakens an intensity of an electric field concentrated at the PN junction in the surface area of the substrate 1, resulting in providing a diode with a high breakdown voltage. Referring to Fig. 2, a P^+ type guard ring region 7 is provided surrounding a P^+ type diffusion area 2 at a given interval therebetween. With this structure, when a depletion layer (as indicated by a dotted line) produced when an inverse bias voltage -V is applied to the anode electrode 4 grows to reach the guard ring region 7, the guard ring region 7 shares a given amount of the voltage, so that an electric field between the diffusion area 2 and the guard ring 7 is kept at a fixed value. An electric field larger than the fixed value is used for further extending the depletion layer beyond the guard ring region 7. Therefore, the concentration of the electric field at the PN junction in the surface area of the substrate 1 is relieved, allowing provision of diodes with a high breakdown voltage. If necessary, a plurality of guard ring regions 7, not a single region, may be provided.

When negative electric charges are attached onto the insulating film, a channel is formed in a part of the surface of the substrate 1 corresponding to the part of the insulating layer with the electric charges attached. The formation of the channel deteriorates the function of the guard ring 7, that is, a function to restrict an electric field between the diffusion region 2 and the guard ring region to a given value. Since an amount of the charge attached to the insulating layer 3 is not always constant, and hence a conductivity of a channel formed by the charge is also not fixed. This results in an instability of an expansion of the

depletion layer. In order to remove the instability, Japanese Patent Publication No. 36513/49 (1974) discloses a semiconductor device with a structure as shown in Fig. 3. In Fig. 3, first and second guard ring regions 7a and 7b are provided surrounding a P^+ type diffusion region 2. A field plate 8a kept at the potential equal to that of the guard ring region 7a and a field plate 8b kept at the potential equal to that of the guard ring region 7b are provided on an insulating layer 3, extending toward a diffusion layer 2. In the structure of the semiconductor device, when an inverse bias voltage is applied to an anode electrode 4, the guard ring regions 7a and 7b share given voltages. Therefore, the electric field concentration at the PN junction in the surface area of the diffusion region 2 is prevented. Further, the field plates 8a and 8b are kept at the potential equal to that of the guard ring regions 7a and 7b. For this reason, the instability of the expansion of the depletion layer due to the charge attachment to the insulating film 3 is prevented, providing stable semiconductor devices with a high breakdown voltage.

The semiconductor device shown in Fig. 3, however, has the following drawbacks. Firstly, there are optimum values in the distances between the diffusion region 2 and the first guard ring region 7a and between the first guard ring region 7a and the second guard ring region 7b. If the distances do not fall within the optimum values, respectively, a high breakdown voltage characteristic can not be obtained. Further, it is difficult to secure the optimum values of the distances in manufacturing the semiconductor devices. Secondly, when a low ON-resistance of the semiconductor device is required, a resistance of the semiconductor substrate 1 must be set small. It is as a matter of course that when the resistance of the substrate is small, the expansion of the depletion layer is small. Meantime, the field plates 8a and 8b are extended in a direction

to interrupt the expansion of the depletion layer. In order that the guard ring regions 7a and 7b share given voltages, the distance between the diffusion layer 2 and the guard ring region 7a and the distance between two guard ring regions must be shortened. This will be discussed in detail. Let us consider a case to manufacture a semiconductor device in which the resistance of the substrate 1 is below 18 Ω·cm and the breakdown voltage is the order of several hundred volts. A thickness of the depletion layer extending from the diffusion layer 2 to the inner side of the substrate 1 when an inverse bias voltage is applied to the anode electrode 4, is small, compared to a case where the substrate 1 has a high resistance. Therefore, a desired high breakdown voltage can not be obtained of course. In order to make the depletion layer expaned from the diffusion layer 2 to the guard ring region 7a before the inverse bias voltage reaches a breakdown voltage at the PN junction, a distance between the diffusion area 2 and the guard ring region 7a must be set small. For the same reason, the distance between the guard ring regions 7a and 7b must be set small. Therefore, the manufacturing of the semiconductor devices is difficult and a production yield of the semiconductor devices is deteriorated.

Accordingly, an object of the present invention is to provide a planar type semiconductor device which has a high breakdown voltage characteristic of about several hundreds V when a resistance of the semiconductor substrate is relatively low and can be manufactured at a good production yield.

A planar type semiconductor device with a high breakdown voltage according to the present invention has a diffusion region of a second conductivity type formed in a selected portion of a surface of a semiconductor layer of a first conductivity type, at least one guard ring region of a second conductivity type formed in the surface of the semiconductor layer, surrounding the

diffusion region at a given distance, and an insulating film covering a given portion of the surface of the semiconductor layer, and is characterized by a first conductive layer which is provided on the insulating film formed outside the diffusion region and is at the potential equal to that of the diffusion area, and by a second conductive layer which is provided on the insulating layer formed outside the guard ring region and is kept at the potential equal to that of the guard ring region.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a partial cross sectional view of a prior PN junction diode with a field plate;

Fig. 2 is a partial cross sectional view of another prior PN junction diode with a guard ring region;

Fig. 3 is a partial cross sectional view of yet another prior PN junction diode with guard ring regions and field plates;

Fig. 4 is a partial cross sectional view of a PN junction diode for explaining the principle of the present invention;

Fig. 5 is a partial cross sectional view of an embodiment when a semiconductor device according to the present invention is applied for a DMOS (double-diffused metal oxide semiconductor) transistor;

Fig. 6 is a cross sectional view of a PN junction diode for theoritically analyzing a characteristic of a semiconductor device according to the present invention.

In Fig. 4 illustrating an embodiment where the present invention is applied to a PN diode, like reference numerals are attached to like portions in Fig. 3. In Fig. 4, on an upper surface of an N type semiconductor substrate 1 having a relatively low resistivity 18 $\Omega \cdot cm$ or less, for example, there are formed a P^+ type diffusion region 2, a first guard ring region 7a surrounding

the diffusion region 2 at a predetermined distance, and a second guard ring region 7b surrounding the region 7a at a predetermined distance. An anode electrode 4 is provided in contact with the diffusion region 2. An extended portion of the anode electrode 4, or a first field plate 9a is provided on an insulating layer 3 provided at the periphery of the diffusion region 2. The electrode in contact with the first guard ring region 7a is extended onto the insulating layer 3 provided outside the region 7a. The extended portion serves as a second field plate 9b. Further, the electrode contacting with the second guard ring region 7b is extended onto the insulating layer 3 provided outside the region 7b and the extended portion serves as a third field plate 9c. The first to third field plates 9a to 9c are extended in a direction which allows a depletion layer produced when an inverse bias voltage is applied to the anode electode 4 to extend outwardly. In the structure shown in Fig. 4, potentials of the field plates 9a to 9c are lower than surface voltages of the substrate 1 right under these field plates. As a result, an extending rate of the depletion layer from the diffusion region 2 toward the outside is larger than that in the case of Fig. 3. Therefore, even when the resistivity of the substrate 1 is small, it is possible to manufacture a semiconductor device having a breakdown voltage of hundreds of volts or so, as a good production yield by allotting predetermined voltages to the guard ring regions 7a and 7b without reducing the distances between the diffusion region 2 and the first guard ring region 7a and between the second and third guard ring regions. Experiment conducted by inventors showed that diodes with a high brakdown voltage of more than 400 V could be manufactured at a high production yield with the structure shown in Fig. 4. Of course, it can solve the disadvantage of the device shown in Fig. 2.

In Fig. 4, it is found that, when the resistivity

of the substrate 1 is relatively low, a potential difference between the diffusion region 2 and the first guard ring region 7a and a potential difference between the first and second guard ring regions are dependent on a thickness of the insulating layer 3, and not dependent on the distances between these regions. The fact will be theoretically analysed later referring to Fig. 6. An actual control of the thickness of the insulating layer 3 is very easy, and the fact that the potential differences are controllable by controlling the thickness makes the design of the semiconductor device remarkably easy. Therefore, the semiconductor devices with a high breakdown voltage may be manufactured at a good production yield.

An embodiment in which the present invention is applied to a DMOS (double-diffused metal oxide semiconductor) transistor with a breakdown of about 450 V and an ON-resistance of about 0.3 Ω, will be described referring to Fig. 5. In Fig. 5, reference numeral 11 designates an N^+ type Si substrate with a low resistivity provided on a drain electrode 21. The N^+ type substrate 11 makes up a drain region. An N type epitaxial layer 12 with resistivity of 12 Ω·cm and a thickness of about 30 to 40 μm is formed on the substrate 11. In the layer 12, P type diffusion layer 13a and 13b serving as channel regions, and N^+ type diffusion layer 14a and 14b serving as source regions are formed. The channel regions and source regions are formed through a double diffusion process by self-alignment. A gate oxide film 15 is provided on the channel regions 22, and a gate electrode 18 is provided on the gate oxide film 15. A P^+ type guard ring region 17 is formed through the diffusion process, surrounding the outside P type diffusion layer 13b. The distance between the P type diffusion region 13b and the guard ring region 17 is about 10 μm. A source electrode 19a is provided contacting with the diffusion region 13a and the N^+ type diffusion layer 14.

A source electrode 19b is in contact with the P type diffusion region 13b and the N^+ type diffusion region 14b, and is extended onto an insulating film 16 provided on the outside of the P type diffusion region 13b. And the extended portion 20a is a first field plate corresponding to the first field plate 9a in Fig. 4. The electrode in contact with the P^+ type guard ring region 17 is extended onto the insulating layer 16 provided on the outside of the region 17. The extended portion 20b is a second field plate corresponding to the second field plate 9b in Fig. 4. The source electrodes 19a and 19b are commonly supplied with a source voltage, and the gate electrode 18 is applied with a gate voltage.

In the case of Fig. 5, a depletion layer extending outwardly from the P type diffusion region 13b easily reaches the guard ring region 17. The electric field between the diffusion region 13b and the guard ring region 17 is held at a substantially constant value, and the breakdown voltage of the DMOS can be made higher also in the case of Fig. 4. In the DMOS transistor having the structure shown in Fig. 5, the breakdown voltage between the drain and source is 450 V or more, and its ON-resistance is 0.3 Ω or less. Besides, the transistor can be manufactured yield rate of 90 % or more. In a DMOS transistor fabricated under the same condition as that of Fig. 5, except that neither field plate 20a nor 20b is provided, a number of the transistors produced had each a less than 450 V breakdown voltage between the drain and source and 50 % or less production yield. According to the present invention, a kind of synergism of the guard ring regions and the field plates reduces the number of the guard ring regions for obtaining a high breakdown voltage. Further, it is not necessary to make extremely small the distances between the diffusion region and the first guard ring region and between the guard ring regions. This implies that the production yield in the manufacturing

process is improved.

Referring to Fig. 6, let us theoretically analyse the fact that the potential difference between the guard ring regions is a function of an impurity concentration N_B of the semiconductor layer with these guard ring regions are provided and a thickness t_{ox} of the insulating layer with the field plates. In Fig. 6, provided in an N^- semiconductor laeyr 30 grounded are a P^+ type diffusion region 31, a P^+ type first guard ring region 32 and a P^+ second guard ring region 33 surrounding the diffusion region. A first field plate 35a intergral with an anode electrode for applying an inverse bias voltage V_M to the P^+ diffusion region 31, a second field plate 35b having the equal voltage to that of the first guard ring region 32 and a third field plate 35c having the equal voltage to that of the second guard ring region 33 are provided on an insulating layer 34 with a thickness t_{ox}, extending in a direction shown in the figure. Reference numeral 36 designates a depletion layer. A voltage difference between the guard rings 32 and 33 is equal to that between the field plates 35b and 35c. Therefore, a voltage V_1 of the first guard ring 32 when the semiconductor layer 30 is grounded is given by an equation (1).

$$|V_1| = |V_2| + V_{ox} \quad \ldots\ldots (1)$$

where reference symbol V_2 indicates a voltage of the second guard ring 33, V_{ox} a voltage across an oxide insulator 34 between the guard ring 33 and the field plate 35b. For ease of the explanation, assuming that a PN junction of the guard ring 33 is flat and let us apply an abrupt flat junction approximation to the PN junction of the guard ring 33. Then, the voltage V_2 of the guard ring 33 is approximately given by an equation (2).

$$|V_2| = \frac{qN_BW^2}{2\varepsilon_{si}} \quad \ldots\ldots (2)$$

where N_B is an impurity concentration of the N^- layer 30, W is a width of the depletion layer under the guard ring 33, ε_{si} is a dielectric constant of the layer 30

and q designates a unit charge. A ratio V_2/V_{ox} is proportional to a ratio of a capacitance of the oxide layer 34 to a capacitance of the depletion layer 36. Therefore, an equation 3 holds.

$$\frac{|V_2|}{V_{ox}} = \left(\frac{\varepsilon_{ox}}{t_{ox}}\right)/\left(\frac{2\varepsilon_{si}}{W}\right) \quad \ldots\ldots (3)$$

where ε_{ox} is a dielectric constant of the oxide layer 34, t_{ox} is a thickness of the oxide layer 36, as described above. Combining the equations 1 to 3, we have equation 4,

$$|V_1 - V_2| = \frac{t_{ox}}{\varepsilon_{ox}}[2\varepsilon_{si}qN_B|V_2|]^{\frac{1}{2}} \quad \ldots\ldots (4)$$

As seen from the equation 4, the potential difference between the first and second guard ring regions are expressed by a function of only the thickness t_{ox} of the insulating layer 34, an impurity concentration N_B of the N^- layer 30 and the voltage V_2 or V_1. This is true for the potential difference between the diffusion region 31 and the first guard ring region 32. In other words, the potential difference does not dependent on the spacing between the diffusion region 31 and the first guard ring region 32 or between the first and second guard ring regions. As already stated, this fact not only extremely simplifies the manufacturing process of the semiconductor devices with a high breakdown voltage, but also greatly improves a production yield of the semiconductor device. The reason for this is that when the semiconductor substrate has a low resistance, there is no need for shortening the distance between the diffusion region and the first guard ring or the guard ring regions to such an degree as to provide a difficulty in manufacturing the semiconductor devices.

It is evident that the present invention is applicable for other semiconductor device such as bi-polar transistors and thyristors.

Claims:

1. A planar type semiconductor device with a high breakdown voltage having a diffusion region of a second conductivity type formed in a selected portion of a surface of a semiconductor layer of a first conductivity type, at least one guard ring region of a second conductivity type formed in the surface of said semiconductor layer, surrounding said diffusion region at a given distance, and an insulating film covering a given portion of the surface of said semiconductor layer, characterized by a first conductive layer (9a, 20a) which is provided on said insulating film (3, 16) formed outside said diffusion region (2, 13) and is at the potential equal to that of said diffusion area, and a second conductive layer (9b, 20b) which is provided on said insulating layer (3, 16) formed outside said guard ring region (7a, 17) and is kept at the potential equal to that of said guard ring region.

2. The planar type semconductor device as claimed in claim 1, characterized in that said diffusion region (2) and said semiconductor layer (1) cooperately make up a diode.

3. The planar type semiconductor device as claimed in claim 1, characterized in that said semiconductor layer (12) of a first conductivity type is formed on another semiconductor layer (11) of a first conductivity type formed on a drain electrode (21) which will serve as a drain region; said diffusion layer (13) of a second conductivity type is formed in said first conductivity semiconductor layer (12); a source region (14) of a first conductivity type is formed in said diffusion layer; and said source region, said drain region and said diffusion layer cooperately make up a DMOS (double-diffused metal oxide semimconductor) transistor.

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FIG. 1

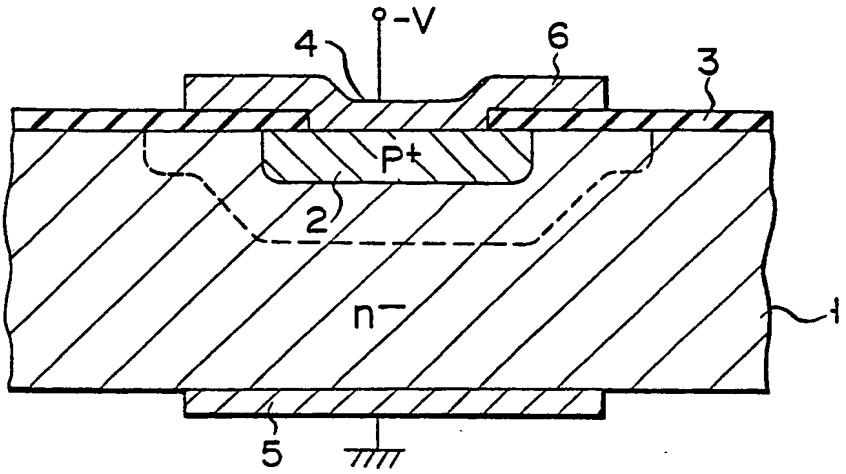

FIG. 2

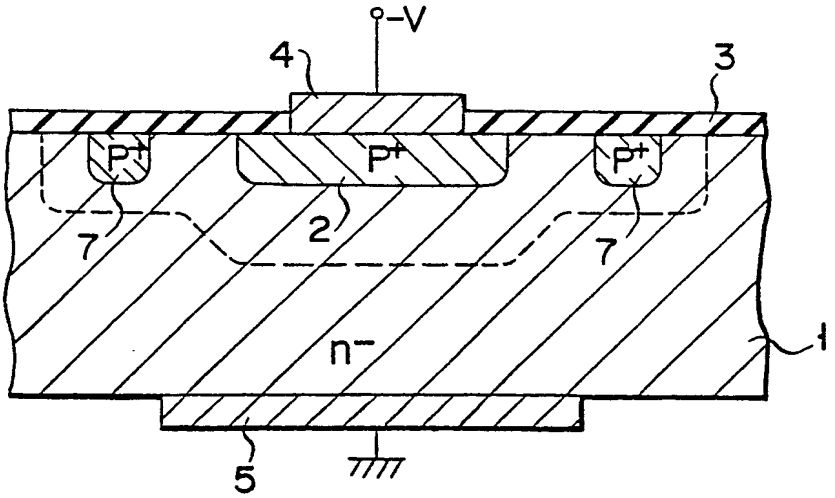

FIG. 3

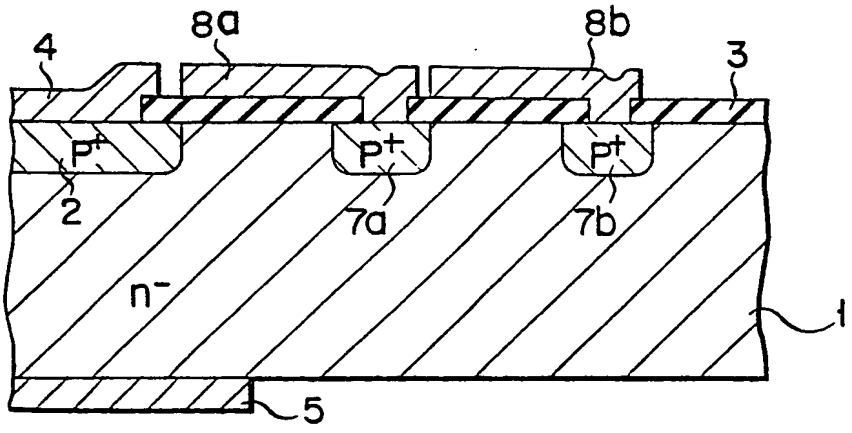

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FIG. 4

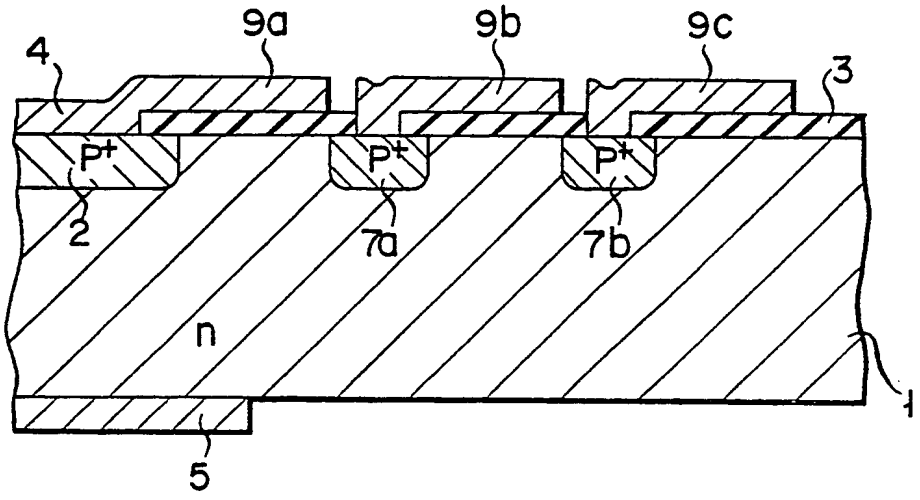


FIG. 6

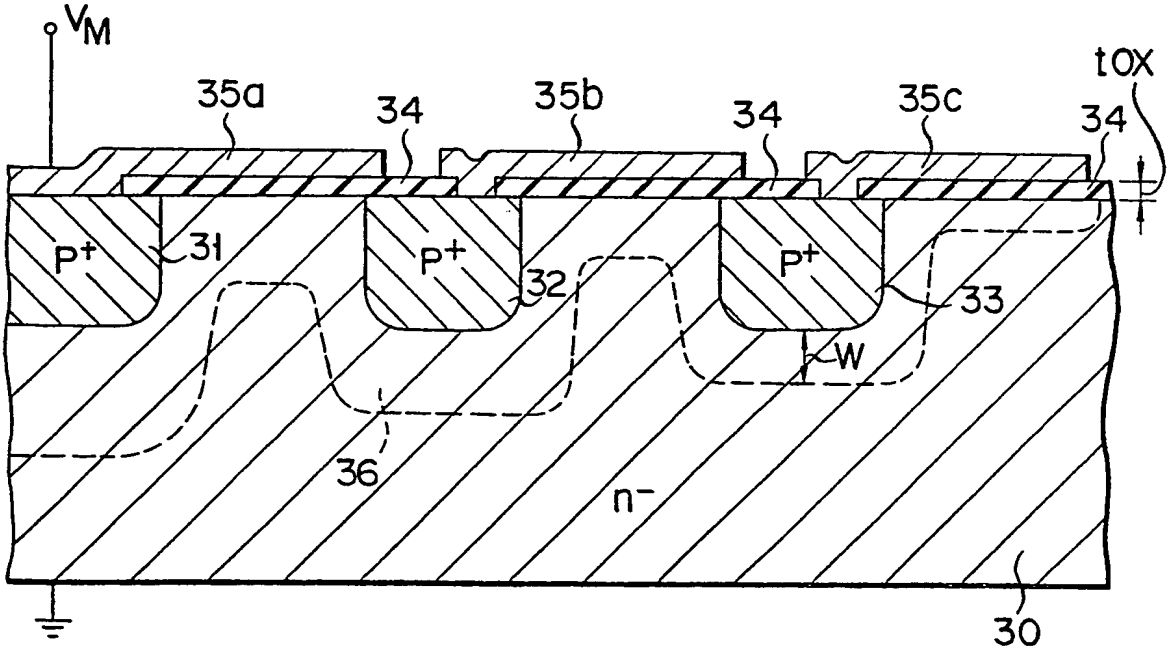
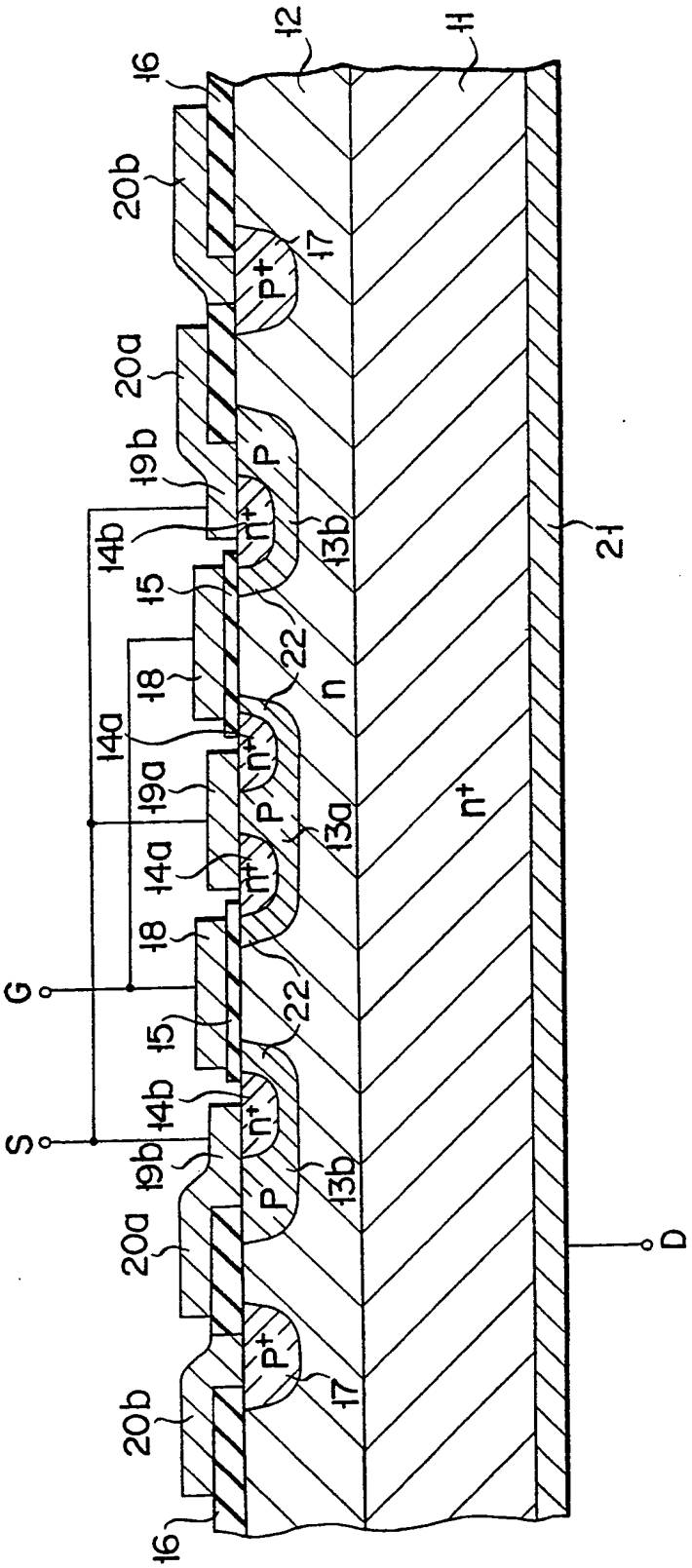


FIG. 5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